

TDMA Noise-Immune DC-DC Boost Converter with Dead-Time Controller for AMOLED Displays

Tae-Un Kim, Ho-Yong Choi Department of Semiconductor Engineering, Chungbuk National University

1. Introduction

DC-DC converters for wearable AMOLED display are required to reduce dead time and TDMA noise.

2.2 Dead time controller



TDMA noise : periodical voltage drop due to TDMA causes overshoot and undershoot of output voltage \rightarrow Degrades AMOLED display quality

Dead time : time interval both NMOS and PMOS turn-off time causes body-diode conduction loss \rightarrow **Decreases power efficiency**

2. Circuit Design

Fig 3. Dead time controller (a) dead time detector, (b) gate driver with dead time controller, (c) waveform of dead time controller, (d) simulation result of dead time controller.

3. Results

Fig 1. Block diagram of proposed DC-DC boost converter.

This paper proposes **TDMA** noise reduction circuit to reduce **TDMA** noise and dead time controller to increase power efficiency

2.1. TDMA Noise Reduction Circuit

• TDMA noise reduction circuit replaces original signal V_{ERROR} to V_{ERROR} R • V_{ERROR} : Original signal generating a reset clock affected by TDMA noise • V_{ERROR R} : New signal generating a reset clock less affected by TDMA noise

- 1. Copies the I_{ERROR} using 1st current mirrors
- 2. Copies the input current using
- 2nd, 3rd current mirrors
- 3. Subtracts *I*_{*IN_Copy2*} from *I*_{*ERROR_Copy*}
- \rightarrow Replaces V_{ERROR} to V_{ERROR_R}

ltem	Summary
Process	0.18 μm BCDMOS
Input voltage	2.9 V ~ 4.4 V
Output voltage	4.6 V
Load Current	1 mA ~ 100 mA
Frequency	0.15 MHz ~ 1 MHz
Output ripple	< 5mV
Chip size	0.7 mm X 1.4 mm

Table 1. Summary of proposed DC-DC converter.

Fig 4. Chip layout.

@ $V_{IN} = 3.7, V_{OUT} = 4.6 V$

Variation of pulse width is reduced \bullet \rightarrow The undershoot and the overshoot V_{SW_N} of output voltage are reduced

> ----- V_{ERROR} @ V_{IN L} with TDMA noise, without TDMA noise reduction circuit ----- V_{ERROR} @ V_{IN H} without TDMA noise, without TDMA noise reduction circuit --- V_{ERROR R} @ V_{IN L} with TDMA noise, with TDMA noise reduction circuit ---- V_{ERROR R} @ V_{IN H} without TDMA noise, with TDMA noise reduction circu (b)

Fig 2. (a) TDMA noise reduction circuit, (b) operation of TDMA noise reduction circuit.

(b)

Fig 5. TDMA noise. (a) boost converter without TDMA noise-reduction circuit, (b) proposed boost converter with TDMA noise-reduction circuit @ I_{LOAD} = 100 mA.

 \rightarrow The undershoot and the overshoot are reduced due to TDMA noise reduction circuit

Fig 6. Power Efficiency.

- TDMA noise reduction circuit reduced undershoot and overshoot by 4 mV, 6 mV.
- The dead time controller controlled to keep dead time at 1 ns.
- Measured power efficiency was 29.6% ~ 76.7%.
- Due to wiring resistance of COB, the converter has low efficiency compared to simulation.

ISD&T Integrated Systems Design & Test Lab. Chungbuk National University

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